TITLE OF THE INVENTION

Semiconductor Package and Method for Producing the Same

BACKGROUND OF THE INVENTION

Field of the Invention

This invention relates to a semiconductor package and a method for producing the same.

Description of Related Art

Up to now, as a semiconductor package, there is an area array BGA (ball grid array) 70 for surface mounting for an LSI (large scale integrated circuit) including a solder ball terminal on its mounting surface to a printed wiring board, as shown in Fig. 1.

This BGA 70 includes a semiconductor device 73, including a first insulating substrate 72 and mounted on this first insulating substrate 72, and a second insulating substrate 75, layered via a prepreg 74 on the first insulating substrate 72, as shown in Fig.1.

The first insulating substrate 72 is a copper-lined layered plate, comprised of e.g., a glass cloth as a base, which is impregnated with an epoxy resin and on both sides of which are bonded copper foils, with the first insulating substrate 72 being formed to substantially a rectangular shape. The first insulating substrate 72 has an electrically conductive pattern 76 formed on its one surface and has a solid pattern for a heat radiation plate 77 formed on its other surface by a print etching method

employing the photolithographic technique. This first insulating substrate 72 includes a mounting portion 79 mounting a semiconductor device 73 at its mid portion. On the rim of the mounting portion 79 of the first insulating substrate 72 is layered a second insulating substrate 75 having an opening 80 for mounting the semiconductor device 73 on the first insulating substrate 72 via a prepreg 74 having an opening 81. The opening 80 is formed by punching the mid portion of the second insulating substrate 75, whilst the opening 81 is formed by punching the mid portion of the prepreg 75. In the first insulating substrate 72, a cavity 82 is formed by this opening 80 and the first insulating substrate 72. On the mounting portion 79 of the first insulating substrate 72 is mounted the semiconductor device 73 with a thermally curable adhesive, such as the die bonding agent 83, through the cavity 82. The semiconductor device 73 is electrically connected with an electrically conductive pattern 76 formed in the first insulating substrate 72 and with the bonding wire 84. The cavity 82 is coated with a liquid encapsulating resin 86 and cured by a thermal process. This planarizes the upper surface of the cavity 82 which is made flush with the upper surface of the second insulating substrate 75 to enable the BGA to be mounted precisely on a motherboard.

On one surface of the second insulating substrate 75, layered on the first insulating substrate 72, there is lined a copper foil which is patterned by a print etching method employing the photolithographic technique to form solder lands 88 and an electrically conductive pattern 89 electrically connecting the solder lands 88. Plural

such solder lands 88 are formed around the opening 80 on one surface of the second insulating substrate 75.

In the second insulating substrate 75, a plated through-hole 91 is bored for extending from the upper surface of the second insulating substrate 75 up to the lower surface of the first insulating substrate 72. Thus, the electrically conductive pattern 89, formed on the second insulating substrate 75, the electrically conductive pattern 76 formed on the first insulating substrate and the solid pattern for the heat radiation plate 77 formed on the other surface of the first insulating substrate are electrically connected via the through-hole 91. With the BGA 70, plural solder balls 92 are formed by printing cream solder on each solder land 88.

On the surface of the first insulating substrate 72 carrying the solid pattern for the heat radiation plate 77, there is bonded a heat radiating plate 93 via an adhesive. This permits heat occasionally stored in the BGA 70 to be dissipated through the heat radiating plate 93 to prevent overheating of the BGA 70.

The BGA 70 is mounted on the motherboard by the solder balls 92 formed on the upper surface of the second insulating substrate 75 to be electrically connected to the electrically conductive layer formed on the motherboard.

Meanwhile, in an electrical equipment, required to be reduced in size and weight, the BGA, enclosed therein, needs to be reduced in size. However, in a package in which an area for a cavity 82 coated with a sealed resin 86 and an area of the second insulating substrate 75, the solder balls 92 and the conductor pattern may be provided

solely on the upper side of the second insulating substrate 75, while they cannot be provided on the cavity 82, thus increasing the package area.

Moreover, since the function of the solder balls and the conductor patterns provide for electrical connection between the semiconductor package and the motherboard, limitations are imposed on reducing the mounting area to render it difficult to reduce the package size.

SUMMARY OF THE INVENTION

It is therefore an object of the present invention to provide a semiconductor package capable of loading solder balls on the encapsulating resin to reduce the package size and a method for the preparation of the semiconductor package.

In one aspect, the present invention provides a semiconductor package including a first insulating substrate carrying a mounting portion for mounting a semiconductor device and a first electrically conductive pattern electrically connected to the semiconductor device, a sidewall section formed upright around the mounting portion of the first insulating substrate, a cavity defined by the first insulating substrate and the sidewall section and encapsulated by resin as the semiconductor device is mounted on the mounting portion and a second insulating substrate provided in the cavity and on the sidewall section and carrying a second electrically conductive pattern electrically connected to the first electrically conductive pattern via through-holes formed in the sidewall section. A solder land is provided at least in the cavity on one surface of the first insulating substrate.

In another aspect, the present invention provides a method for the preparation of a semiconductor package comprising the steps of forming a mounting portion for mounting a semiconductor device and a first electrically conductive pattern for electrically connecting the semiconductor device on a first insulating substrate, layering a spacer having an opening of substantially the same size as the mounting portion in one surface of the first insulating substrate, mounting a semiconductor device in the mounting portion defined by the first insulating substrate and the opening provided in the spacer, encapsulating the cavity with encapsulating resin after mounting the semiconductor device in the mounting portion, layering a second insulating substrate carrying the electrically conductive layer on one surface thereof on the spacer, forming a through-hole for establishing electrical connection between the first electrically conductive pattern and the electrically conductive layer, and forming a solder land at least in the cavity in the electrically conductive layer.

In the semiconductor package and the method for the preparation thereof, according to the present invention, in which the electrical wiring can be provided on the resin-encapsulated area of the resin-encapsulated semiconductor device, it is possible to have the solder balls for conduction and connection between the BGA and the motherboard as a portion of the wiring mounted on the resin-encapsulated area of the resin-encapsulated semiconductor device. The result is that the resin-encapsulated cavity represents an effective area in mounting the BGA on the motherboard. Consequently, the semiconductor package is not increased in area so that it is possible

to provide a small-sized semiconductor package with high heat radiation.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig.1 is a cross-sectional view showing a conventional BGA.

Fig.2 is a cross-sectional view showing a BGA embodying the present invention.

Fig.3 is a plan view showing a BGA embodying the present invention.

Fig.4 is a bottom plan view of a BGA embodying the present invention.

Fig.5 is a plan view showing an insulating substrate carrying a land and a conductor pattern.

Fig.6 is a cross-sectional view showing the manner in which a prepreg and an insulating substrate are layered on the insulating substrate to form a sidewall section.

Fig.7 is a plan view showing an insulating substrate carrying a sidewall section.

Fig.8 is a cross-sectional view showing the manner of loading a semiconductor device in a cavity.

Fig.9 is a plan view showing the manner of connecting a semiconductor device to a conductor pattern by a bonding wire.

Fig.10 is a cross-sectional view showing an encapsulating resin in a cavity accommodating a semiconductor device therein.

Fig.11 is a cross-sectional view showing the manner of layering insulating substrates for forming a plated through-hole in the insulating plate, sidewall section and in the insulating substrate.

Fig.12 is a plan view showing the insulating plate shown in Fig.11.

Fig.13 is a plan view showing the manner of forming a through-hole land, a solder land and a conductor pattern in the insulating plate.

Fig.14 is a bottom plan view showing a BGA carrying a solid pattern for a heat radiation plate.

Fig.15 is a cross-sectional view showing the BGA to which is bonded the hear radiating plate.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Referring to the drawings, a BGA to which is applied a semiconductor package embodying the present invention will be explained in detail. Figs.2 to 4 show a BGA 1 embodying the present invention. This BGA 1 is an area array type package for surface mounting an LSI on one entire surface of which plural solder lands are arranged in a lattice. This BGA 1 includes a first insulating substrate 5, having mounted thereon a semiconductor device 2 and having formed thereon an electrically conductive pattern 4, a sidewall section 6 formed upright around a mounting portion 3, a cavity 7 defined by the first insulating substrate 5 and the sidewall section 6, a second insulating substrate 10 on which to form solder lands 9, and a heat radiating plate 11 for preventing overheating of the BGA 1. Within the cavity 7 of the BGA 1 is mounted the semiconductor device 2 and charged an encapsulating resin 12.

The first insulating substrate 5, on which is loaded the semiconductor device 2, is a substantially recording copper-lined laminated plate comprised of a glass cloth as a base material impregnated with an epoxy resin. On both sides of the first insulating

substrate 5 are stuck copper foils. The first insulating substrate 5 is patterned by a print etching method employing the photolithographic technique, whereby an electrically conductive pattern 4 for electrically connecting the mounting portion 3 for mounting the semiconductor device 2 to the semiconductor device 2 mounted around the mounting portion 3 is formed on its one surface. In similar manner, a heat dissipating pattern 15 for radiating the heat from within the package through a heat radiating plate 11 and a land 16 for the through-hole are formed in the first insulating substrate 5.

The mounting portion 3, on which to mount the semiconductor device 2, is provided at a mid portion of the first insulating substrate 5. The semiconductor device 2 is mounted on the mounting portion 3 using a adhesive, such as a die bond, as later explained. The electrically conductive pattern 4, formed around the mounting portion 3, is made up of a land 21 formed continuously around the rim of one surface of the first insulating substrate 5 and patterns 22 formed towards the mounting portion 3 from the land 21 so as to be electrically connected to a bonding wire 13 as later explained. In the land 21 is formed a plated through-hole 26, which will be explained subsequently.

On the other surface of the first insulating substrate 5 is formed a solid pattern for a heat radiation plate 15 to a substantially square shape beginning from the center towards the rim of the first insulating substrate 5. A through-hole land 16, passed through by the plated through-hole 26, is provided around the solid pattern for a heat

radiation plate 15.

The sidewall section 6, formed upright around the first insulating substrate 5, is made up of the prepreg 17 and a spacer substrate 18 layered on the prepreg 17.

The prepreg 17, which unifies the spacer substrate 18 and the first insulating substrate 5 together, has a substantially square-shaped center opening 19 substantially coextensive as the mounting portion 3, and is formed to substantially a square shape of the same size as that of the first insulating substrate 5. This prepreg 17 is layered on the land 21 around the rim of the first insulating substrate 5 and operates as an adhesive layer for the spacer substrate 18 and the first insulating substrate 5. Similarly to the prepreg 17, the spacer substrate 18 has a substantially square-shaped center opening 23 substantially coextensive as the mounting portion 3, and is formed to substantially a square shape of the same size as that of the first insulating substrate 5. This spacer substrate 18 is layered through the prepreg 17 around the rim of the first insulating substrate 5. This forms the cavity 7 of a depth sufficient to hold the semiconductor device 2 in an area surrounded by the sidewall section 6. The cavity 7 exposes the mounting portion 3 provided on the first insulating substrate 5 to outside.

In the sidewall section 6, there are formed plural plated through-holes 26 for extending in the upstanding direction of the sidewall section 6 so as to be passed through an area between a through-hole land 25 formed in continuation to the rim of the layered second insulating substrate 10 and the land 21 formed in continuation on the rim of the first insulating substrate 5.

On the mounting portion 3 provided in the first insulating substrate 5, exposed to outside through the cavity 7 formed in the first insulating substrate 5, a chip-shaped semiconductor device 2 carrying a pre-set electrical circuit is mounted with a thermosetting adhesive, for example, a die-bond agent 27. The semiconductor device 2 and the patterns 22 of the electrically conductive pattern 4 formed on the first insulating substrate 5 are electrically connected to each other by the bonding wire.

The cavity 7, accommodating the semiconductor device 2 therein, is charged with the encapsulating resin 12 so that its upper surface is flush with the sidewall section 6. The encapsulating resin 12 is a liquid thermosetting resin and is cured on heat treatment. This planarizes the upper surface of the BGA 1 to permit the second insulating substrate 10 to be layered positively thereon.

The second insulating substrate 10, layered on the upper surface of the spacer substrate 18, is comprised of a copper-lined layered plate comprised of a glass cloth impregnated with an epoxy resin and on one surface of which is bonded a copper foil. This second insulating substrate 10 is patterned to form solder lands 9, forming solder balls 8, through-hole lands 25 formed with the plated through-holes 26 and a conductor pattern 31 electrically interconnecting the solder lands 9 and the through-hole lands 25 by a print etching method employing the photolithographic technique. The second insulating substrate 10 is layered on the sidewall section 6 and on the cavity 7 through the prepreg 28 so that its patterned surface faces outwards.

The solder lands 9 are formed as a lattice on the entire surface of the second

insulating substrate 10. On the solder lands 9, solder balls 9 for providing for interconnection between the motherboard and the BGA 1 are formed by printing and reflow of a solder cream.

On the opposite side of the first insulating substrate 5 is formed the heat radiating plate 11 for radiating the heat of the BGA 1 to outside to prevent overheating of the BGA 1. The heat radiating plate 11 is bonded, with an adhesive 32, to the solid pattern for a heat radiation plate 15 and to the through-hole lands 16 formed on one surface of the first insulating substrate 5. Thus, in the BGA 1, the heat within the package can be dissipated through the heat radiating plate 11 to outside to prevent malfunctions otherwise caused by overheating.

The BGA 1 is connected to the motherboard by reflow soldering with the solder balls 8 mounted on the second insulating substrate 10 compressing against the mounting surface on the motherboard. This electrically connects the BGA 1 to the motherboard through the solder balls 8 formed on the second insulating substrate 10, conductor pattern 31 and the plated through-holes 26.

With the BGA according to the present invention, in which the wiring can be made on an upper portion of the resin encapsulated area of the resin-encapsulated semiconductor device, the solder balls 8 for providing for electrical interconnection between the BGA 1 and the motherboard as part of the wiring can be installed in the encapsulated area of the semiconductor device 2 of the BGA 1. Consequently, the resin-encapsulated cavity represents an area effective for mounting, without proving

a dead space in connecting the BGA to the motherboard. So, the package area is not increased to realize a small-sized high heat dissipating BGA.

The above-described BGA 1 can be prepared as follows:

First, copper foils are bonded to both sides of a glass cloth impregnated with the epoxy resin to form the first insulating substrate 5 comprised of copper-lined laminated sheets. Then, as shown in Fig.5, the first insulating substrate 5 is formed to a substantially rectangular form. Using a photo film, having printed thereon a pattern registering with the lands 21 and the patterns 22, one surface of the first insulating substrate 5 is patterned by a print etching method employing the photolithographic technique. This forms the electrically conductive pattern 4, comprised of the lands 21, formed for extending along the rim of the first insulating substrate 5, and the patterns 22, formed for extending from these lands 21 to the mounting portion 3 formed at a mid portion of the first insulating substrate 5. The opposite side of the first insulating substrate 5 is lined in its entirety with a copper pattern 20.

In a similar manner, the substantially recording prepreg 17 and the spacer substrate 18 are formed and mid portions of the prepreg 17 and the spacer substrate 18 are punched off to form the openings 19, 23.

Then, as shown in Figs.6 and 7, the spacer substrate 18 of the same size as the first insulating substrate 5 is layered over the lands 21 through the spacer substrate 18 and unified to the first insulating substrate 5 by vacuum hot pressing to form the

sidewall section 6. The cavity 7 then is formed by the sidewall section 6 being formed on its rim.

The semiconductor device 2, carrying the electrical circuitry, is loaded in the cavity 7, as shown in Fig.8. This semiconductor device 2 is loaded on the mounting portion 3, formed at a mid portion of the first insulating substrate 5, through an adhesive, such as a die bond 27. The semiconductor device 2 then is wired with the bonding wire by a wire bonding device, not shown.

Then, as shown in Fig.10, the liquid encapsulating resin 12 is applied to the cavity 7 accommodating the semiconductor device 2. This encapsulating resin 12 is the thermosetting resin, such as epoxy, melamine, phenol or urea, and is cured by a heat treatment process, not shown. In this manner, the encapsulated area of the semiconductor device 2 of the BGA 1 is made substantially flush with the upper surface of the sidewall section 6. Meanwhile, in the BGA 1, the upper surface of the sidewall section 6 is made flush with the encapsulated area by appropriately polishing the upper surface of the sidewall section 6 or the cured encapsulating resin 12.

The second insulating substrate 10 of the same size as the first insulating substrate 5 then is layered to cover the sidewall section 6 and an area coated with the encapsulating resin 12. This second insulating substrate 10 is a laminated sheet, lined with copper on its one surface. Specifically, the second insulating substrate 10 is a glass cloth, impregnated with the epoxy resin, one surface of which is lined with a copper foil. The second insulating substrate 10 is layered via a prepreg 28 of the same

size as the first insulating substrate 5, with a surface lined with the copper foil facing outwards, and unified to the first insulating substrate 5 on vacuum hot pressing.

Then, as shown in Figs.11 and 12, a series of through-holes traversing both sides of the sidewall section 6 and the first insulating substrate 5 are formed for extending along the rim of the second insulating substrate 10, using an NC ball lathe. These through-holes are deburred by desmearing such as sulfuric acid method, chromic acid method or the plasma method. The through-holes 26 then are plated by electrolytic plating or non-electrolytic plating to form the plated through-holes 26. These through-holes 26, traversing the lands 21 formed in the first insulating substrate 5, provide for interconnection of the electrically conductive pattern 4 formed on the first insulating substrate 5, the second insulating substrate 10 and the copper pattern 20 deposited on the opposite surface of the first insulating substrate 5.

The second insulating substrate 10 then is patterned to form the solder lands 9, through-hole lands 25 and the conductor patterns 31 on its surface carrying the copper foil by a print etching method employing the photolithographic technique with the aid of the photo film carrying the solder lands 9, through-hole lands 25 and the conductor patterns 31 interconnecting the solder lands 9 and the through-hole lands 25, as shown in Fig.13. The through-hole lands 25 are formed so that the plated through-holes 26 formed in succession along the rim of the second insulating substrate 10 will be at the center of the lands, as shown in Fig.13. These solder lands 9 and the through-hole lands 25 are connected to each other each by a sole conductor pattern 31.

In similar manner, a series of the through-hole lands 16 are formed along the solid pattern for a heat radiation plate 15 and the first insulating substrate 5 in the copper pattern 20 formed on the opposite surface of the first insulating substrate 5, as shown in Fig.14. Similarly to the through-hole lands 25, the through-hole lands 16 are formed so that the plated through-holes 26 will be at the center of the lands. The solid pattern for a heat radiation plate 15 is formed to substantially a square shape extending from the center towards the rim.

On the opposite surface of the first insulating substrate 5, the heat radiating plate 11 is affixed, via an adhesive 32, to overlie the through-hole lands 16 and the solid pattern for the heat radiation plate 15, as shown in Fig.15. This heat radiating plate is of the same size as the first insulating substrate 5. In this manner, the BGA 1 is able to dissipate the heat in the package to outside through the heat radiating plate 11 to prevent malfunctions otherwise produced by overheating.

Then, as shown in Figs.2 and 3, the solder balls 8 for interconnecting the BGA 1 to the motherboard are loaded on the solder lands 9, using a solder ball mounter or a reflow furnace, not shown, to complete the BGA 1, as shown in Figs.2 and 3.

With the above-described manufacturing method for the BGA, since the wiring can be formed on top of the resin encapsulating area of the resin-encapsulated semiconductor device, the solder balls 8 providing for connection between the BGA 1 and the motherboard can be installed in the encapsulating area of the resin-encapsulated semiconductor device 2. So, the encapsulated cavity portion represents

an area effective for mounting without proving a dead space for the connection of the BGA to the motherboard, so that the package area is not increased to provide a small-sized BGA with high heat radiation.

Meanwhile, the various conductor patterns formed in the first insulating substrate 5 and in the second insulating substrate 10 can be formed by any known suitable printing method; such as screen printing method, in addition to the print etch method employing the photolithographic technique.